In the Claims:

1. (Currently Amended) A memory system comprising:

a circuit board having a first means for receiving and a second means for receiving;

a first signal bus portion on said circuit board connected to said first means for receiving; and

a second signal bus portion on said circuit board connected to said second means for receiving and not connected to said first signal bus portion,

a first memory module received in said first means for receiving;

a second memory module received in said second means for receiving; and

a flexible bridge connecting said first and second memory modules for providing a signal bus between said memory modules, so that said first and second memory modules are serially connected between said first and second signal bus portions.

2. (Original) The memory system of claim 1, wherein the memory modules are received in the respective means for receiving at a first side thereof and wherein the flexible bridge extends from a respective second side of the memory modules.

3. (Original) The memory system of claim 1, wherein the respective second side of the memory module is arranged opposite to the first side thereof.

4. (Currently Amended) The memory system of claim 1, wherein the receiving means are [[slots ]]slot connectors for receiving memory modules adapted for DDR memory systems.

5. (Original) The memory system of claim 1, wherein the flexible bridge comprises data lines and/or control signal lines for providing a data bus and/or a control signal bus between said memory modules.

6. (Currently Amended) The memory system of claim 1, wherein a memory controller ~~and signal lines are~~ is provided on said circuit board and connected to said first signal bus portion, wherein said first signal bus portion ~~lines provide~~ provides a data bus and/or a control signal bus between said controller and said first memory module.

7. (Currently Amended) The memory system of claim 6, wherein said first signal bus portion ~~lines on said circuit board further provide~~ provides a clock bus between said memory controller and said first memory module.

8. (Currently Amended) The memory system of claim [[6]]1, further comprising ~~a third memory module received in a~~ third means for receiving on said circuit board and wherein said second signal bus portion connects said second means for receiving to said third means for receiving ~~signal lines on said circuit board further provide a data bus and/or a control signal bus between said second and said third memory modules~~.

9. (Original) The memory system of claim 1, wherein the bridge is a flexible printed circuit board having a ground layer and a signal layer.

10. (Currently Amended) The memory system of claim 1, wherein said signal bus provided by said flexible bridge has a trace impedance matched ~~adapted~~ to a trace impedance of said bus portions ~~buses~~ on the ~~memory module and the~~ circuit board and matched to a trace impedance of bus portions on said memory modules ~~to which said signal bus is connected~~.

11. (Canceled)

12. (New) The memory system of claim 1, wherein the circuit board comprises four means for receiving and wherein the flexible bridge has a length permitting the first and second means for receiving to be separated by two other means for receiving.

13. (New) The memory system of claim 1 wherein said first and second receiving means are first and second slot connectors each for receiving a single memory module.

14. (New) A memory system comprising:

a circuit board having a first slot connector for receiving a single memory module and a second slot connector for receiving a single memory module;

a first signal bus portion on said circuit board connected to said first slot connector;

a second signal bus portion on said circuit board having a first end connected to said second slot connector and not connected to said first signal bus portion;

a first memory module mounted in said first slot connector;

a second memory module mounted in said second slot connector; and

a flexible bridge connecting said first and second memory modules for providing a signal bus between said memory modules.

15. (New) The memory system of claim 14, wherein the memory modules are received in the respective slot connectors at a first side thereof and wherein the flexible bridge extends from a second side of the memory modules.

16. (New) The memory system of claim 14, wherein the flexible bridge comprises data lines and/or control signal lines for providing a data bus and/or a control signal bus between said memory modules.

17. (New) The memory system of claim 14 further comprising a third slot connector and a fourth slot connector.

18. (New) The memory system of claim 17 wherein said third and fourth slot connectors are located between said first and second slot connector.

19. (New) The memory system of claim 17, wherein the other end of said second signal bus portion is connected to said third slot connector and further comprising a third signal bus portion on said circuit board connected to said fourth slot connector;

a third memory module mounted in said third slot connector;

a fourth memory module mounted in said fourth slot connector;

another flexible bridge connecting said third and fourth memory modules to provide a signal bus between said third and fourth memory modules so that said third and fourth memory modular are serially connected between said second and third signal bus portions and so that said first, second, third, and fourth memory modules are serially connected between said first and third bus portions.

20. (New) A memory system comprising:

a circuit board comprising a first slot connector and a second slot connector, each of said first and second slot connectors capable of receiving only a single memory module;

a first memory module mounted in said first slot connector;

a second memory module mounted in said second slot connector; and

a flexible bridge connecting said first and second memory module for providing a signal bus between said memory modules.